

TRANSMITTAL LETTER
(General - Patent Pending)

Docket No.
BUR920040001US1 (17382)

In Re Application Of: **John M. Cohn, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/709,754	May 24, 2004	John P. Trimmings	23389	2117	3753

Title: **A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

RESPONSE UNDER 37 C.F.R. §§1.111 AND 1.143

in the above identified application.

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Dated: **August 9, 2007**

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